



G31T-A

V:1.0

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REVISION HISTORY:

Rev	Date	Notes
A	2007-09-17	
1.0	2007-11.16	

IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.



3) DESIGN NOTES in red are critical, and must be understood and followed.

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

Elitegroup Computer Systems	
Title Cover Sheet	
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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	20	F/G/H/C	PREQ-3	PGNT-3
PCI2	21	G/H/C/D	PREQ-4	PGNT-4
PCI3	17	C/D/E/F	PREQ-0	PGNT-0
PCI4	18	D/E/F/G	PREQ-1	PGNT-1
PCI5	19	E/F/G/H	PREQ-2	PGNT-2

VCORE POWER
PWM VRD11
(RT8802A)

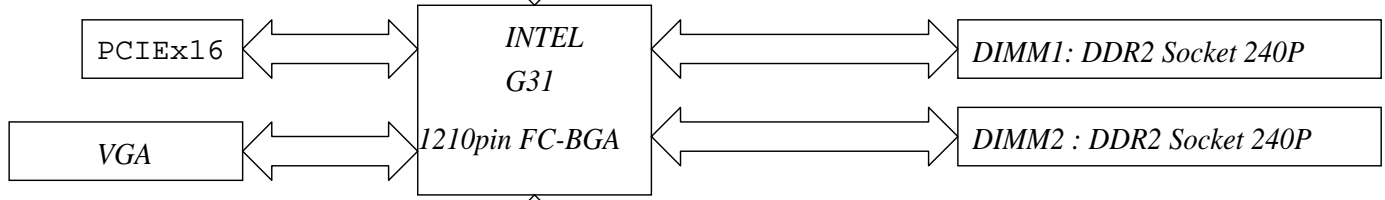
INTEL
P4 Processor
Core 2 Duo & Wolfdale
LGA 775 pin

CLOCK GEN:9LPRS509

PCB : 305x200 mm ; 4 layers

FSB : 1333MHz & Freq : 333MHz
FSB : 1066MHz & Freq : 266MHz

BW : 10.7GB/s @ DDR2 :800/667MHz



Analong Display
RAMDAC: 400MHz
Resolutions Up To 2048x1536@75Hz


Line in
Line out
Mic in
Center/Bass out
Surround
Side-Surround

Audio Codec
ALC662/883

SATA1 7Pin
SATA2 7pin
SATA3 7Pin
SATA4 7pin

Flash Bios

Super I/O
ITE 8718F
128pin PQFP

**Elitegroup Computer Systems**

Title
System Block Diagram

Size
B

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VCCP

VCCP

AA8	VCC0
AB3	VCC1
AC2	VCC2
AC24	VCC3
AC25	VCC4
AC26	VCC5
AC27	VCC6
AC28	VCC7
AC29	VCC8
AC30	VCC9
AC8	VCC10
AD23	VCC11
AD24	VCC12
AD25	VCC13
AD26	VCC14
AD27	VCC15
AD28	VCC16
AD29	VCC17
AD30	VCC18
AE11	VCC19
AE12	VCC20
AE14	VCC21
AE15	VCC22
AE16	VCC23
AE17	VCC24
AE19	VCC25
AE21	VCC26
AE22	VCC27
AE23	VCC28
AE24	VCC29
AE25	VCC30
AE12	VCC31
AE14	VCC32
AE15	VCC33
AE16	VCC34
AE17	VCC35
AE21	VCC36
AE22	VCC37
AE8	VCC38
AE9	VCC39
AG11	VCC40
AG12	VCC41
AG14	VCC42
AG15	VCC43
AG18	VCC44
AG19	VCC45
AG21	VCC46
AG22	VCC47
AG25	VCC48
AG28	VCC49
AG29	VCC50
AG30	VCC51
AG8	VCC52
AG9	VCC53
AG11	VCC54
AG12	VCC55
AG14	VCC56
AG15	VCC57
AG18	VCC58
AG19	VCC59
AG21	VCC60
AG22	VCC61
AG25	VCC62
AG28	VCC63
AG29	VCC64
AG30	VCC65
AG8	VCC66
AG9	VCC67
AG11	VCC68
AG12	VCC69
AG14	VCC70
AG15	VCC71
AG18	VCC72
AG19	VCC73
AG21	VCC74
AG22	VCC75
AG25	VCC76
AG28	VCC77
AG29	VCC78
AG30	VCC79
AG8	VCC80
AG9	VCC81
AG11	VCC82
AG12	VCC83
AG14	VCC84
AG15	VCC85
AG18	VCC86
AG19	VCC87
AG21	VCC88
AG22	VCC89
AG25	VCC90
AG28	VCC91
AG29	VCC92
AG30	VCC93
AK8	VCC94
AK9	VCC95
AK11	VCC96
AK12	VCC97
AK14	VCC98
AK15	VCC99
AK18	VCC100
AK19	VCC101
AK21	VCC102
AK22	VCC103
AK25	VCC104
AK28	VCC105
AK8	VCC106
AK9	VCC107
AK11	VCC108
AK12	VCC109
AK14	VCC110
AK15	VCC111
AK18	VCC112
AK19	VCC113
AK21	VCC114
AK22	VCC115
AK25	VCC116
AK28	VCC117
AK8	VCC118
AK9	VCC119
AK11	VCC120
AK12	VCC121

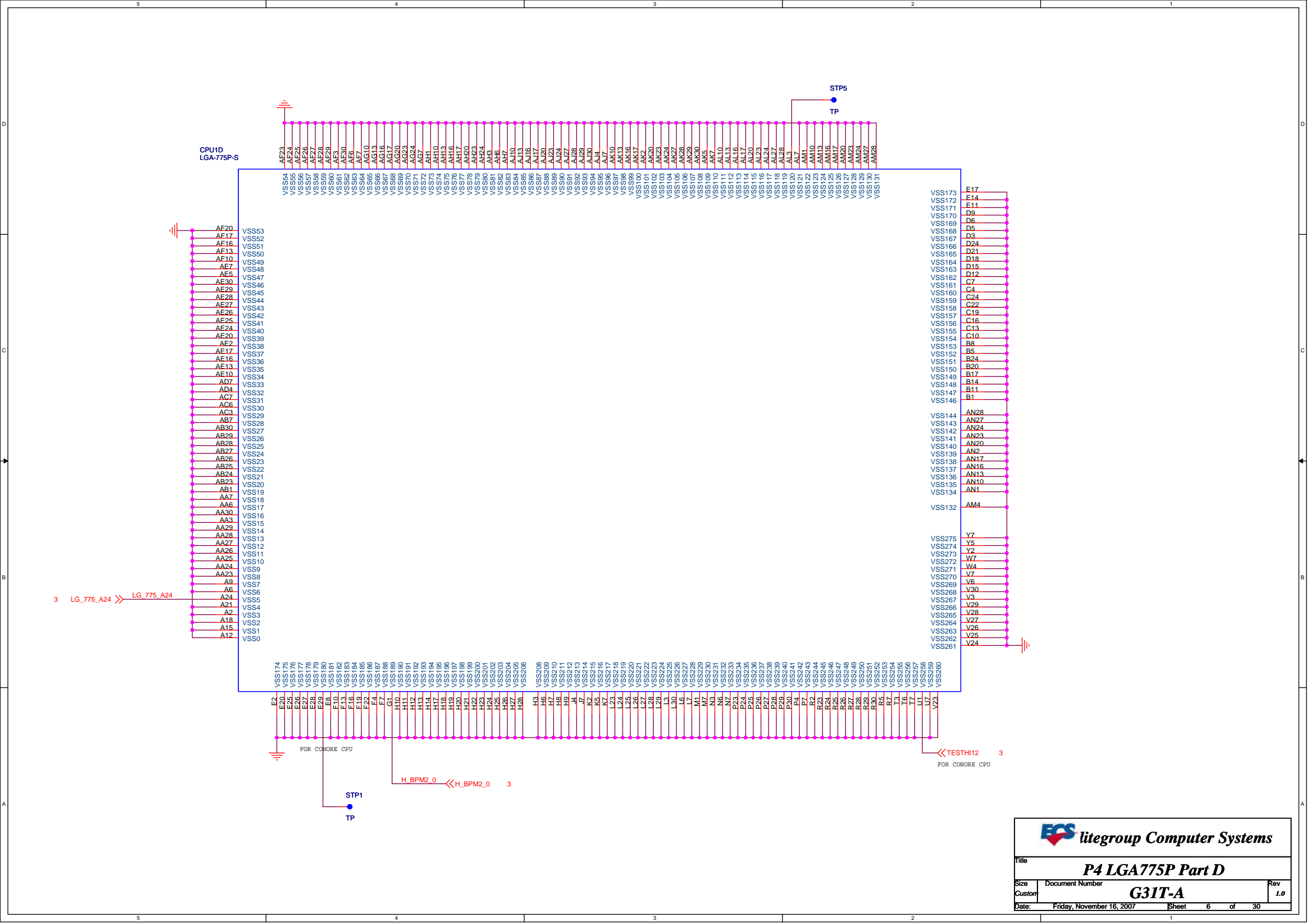
CPU1C
LGA-775P-S

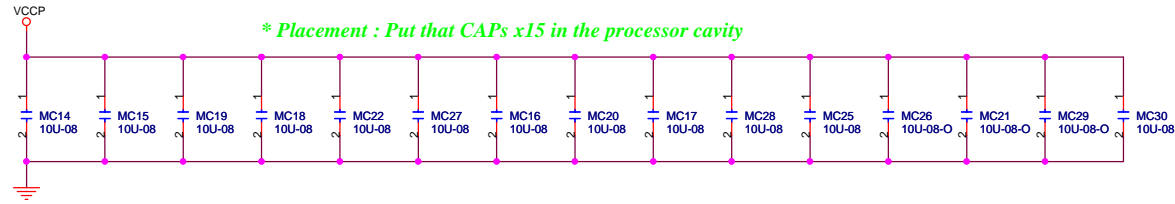
AM8	VCC122
AM9	VCC123
AN11	VCC124
AN14	VCC125
AN15	VCC126
AN18	VCC127
AN19	VCC128
AN21	VCC129
AN22	VCC130
AN25	VCC131
AN26	VCC132
AN29	VCC133
AN30	VCC134
AN8	VCC135
AN9	VCC136
AN11	VCC137
J10	VCC138
J11	VCC139
J12	VCC140
J14	VCC141
J15	VCC142
J18	VCC143
J19	VCC144
J21	VCC145
J22	VCC146
J23	VCC147
J24	VCC148
J25	VCC149
J26	VCC150
J27	VCC151
J28	VCC152
J29	VCC153
J30	VCC154
J31	VCC155
J32	VCC156
J33	VCC157
J34	VCC158
K23	VCC159
K24	VCC160
K25	VCC161
K26	VCC162
K27	VCC163
K28	VCC164
K29	VCC165
K30	VCC166
K8	VCC167
K9	VCC168
M24	VCC169
M25	VCC170
M26	VCC171
M27	VCC172
M28	VCC173
M29	VCC174
M30	VCC175
M31	VCC176
M8	VCC177
N23	VCC178
N24	VCC179
N25	VCC180
N26	VCC181
N27	VCC182
N28	VCC183
N29	VCC184
N30	VCC185
P8	VCC186
P9	VCC187
R8	VCC188
T23	VCC189
T24	VCC190
T25	VCC191
T26	VCC192
T27	VCC193
T28	VCC194
T29	VCC195
T30	VCC196
U23	VCC197
U24	VCC198
U25	VCC199
U26	VCC200
U27	VCC201
U28	VCC202
U29	VCC203
U30	VCC204
U31	VCC205
U8	VCC206
W23	VCC207
W24	VCC208
W25	VCC209
W26	VCC210
W27	VCC211
W28	VCC212
W29	VCC213
W30	VCC214
W8	VCC215
Y23	VCC216
Y24	VCC217
Y25	VCC218
Y26	VCC219
Y27	VCC220
Y28	VCC221
Y29	VCC222
Y30	VCC223
Y8	VCC224
Y9	VCC225



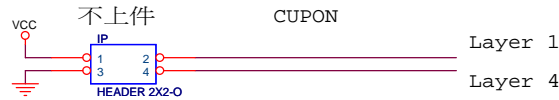
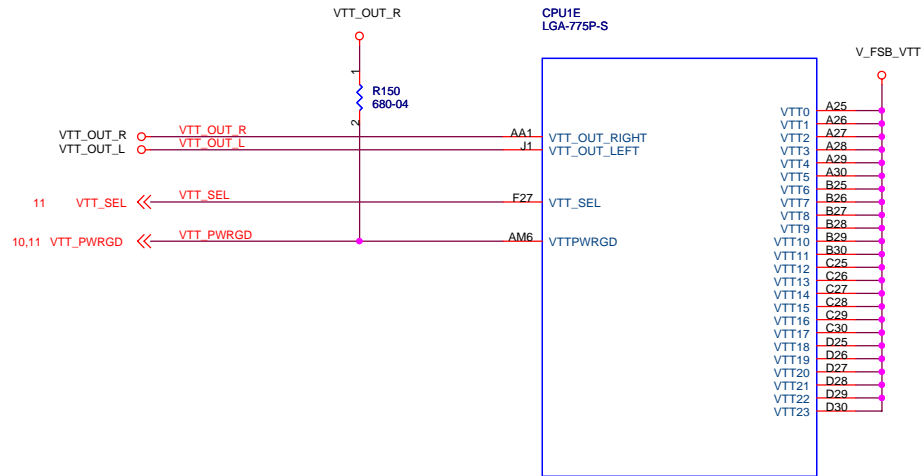
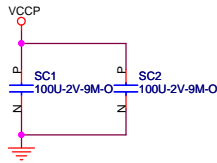
Elitegroup Computer Systems

Title			P4 LGA775P Part C		
Size	Document Number				Rev
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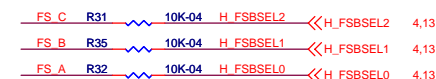
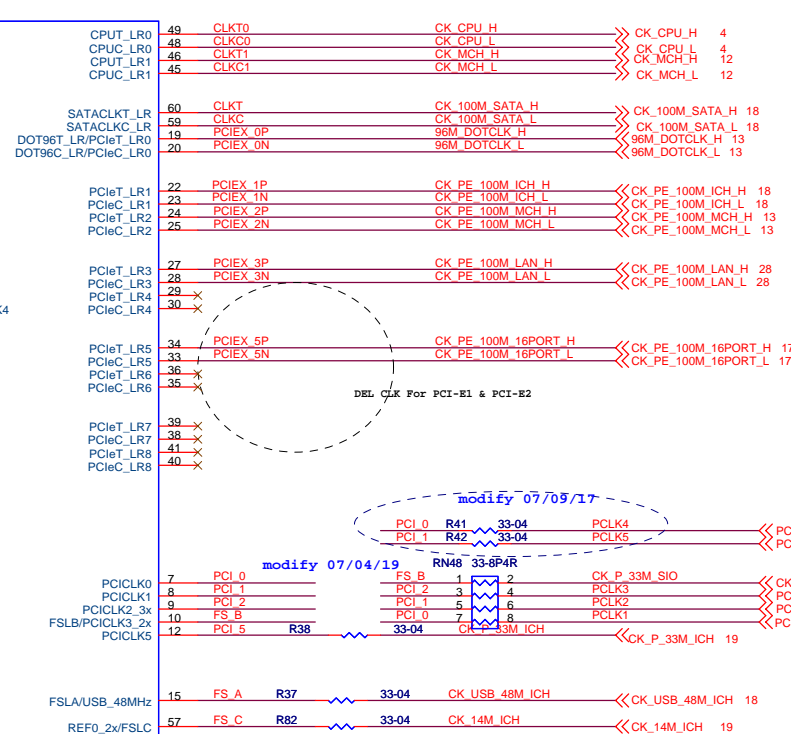
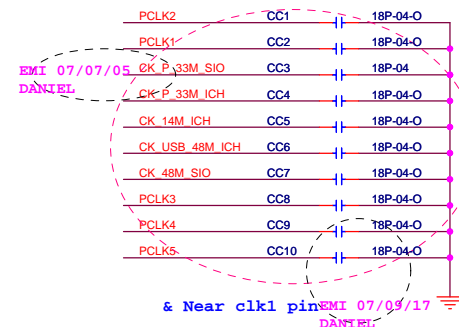
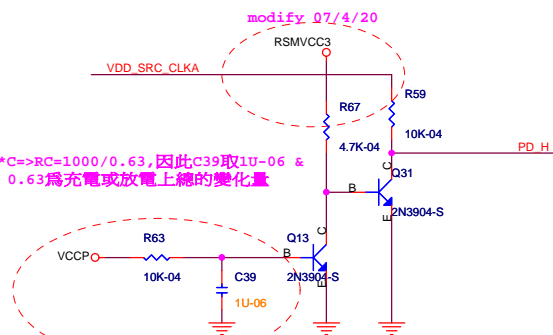
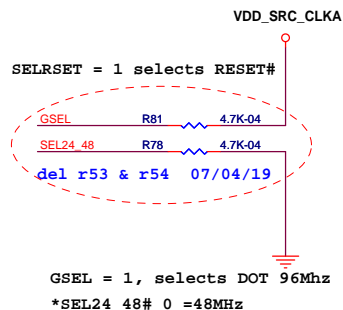
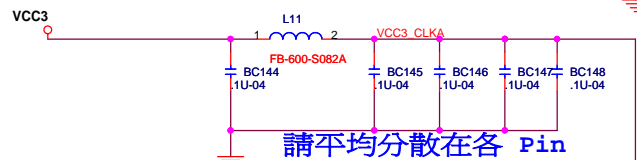




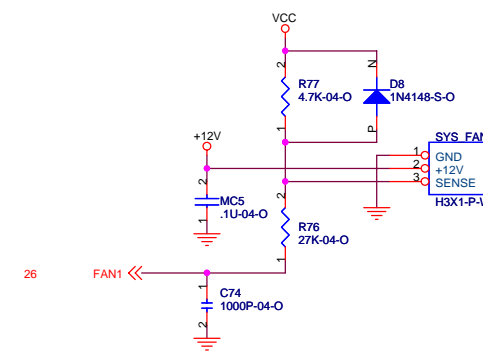
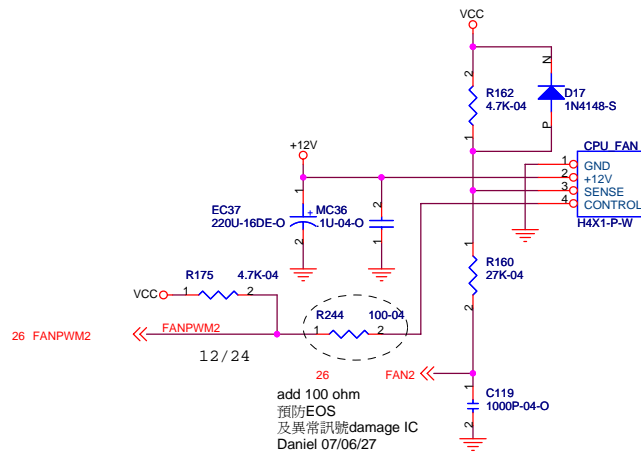
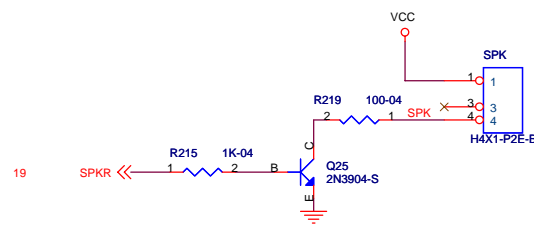
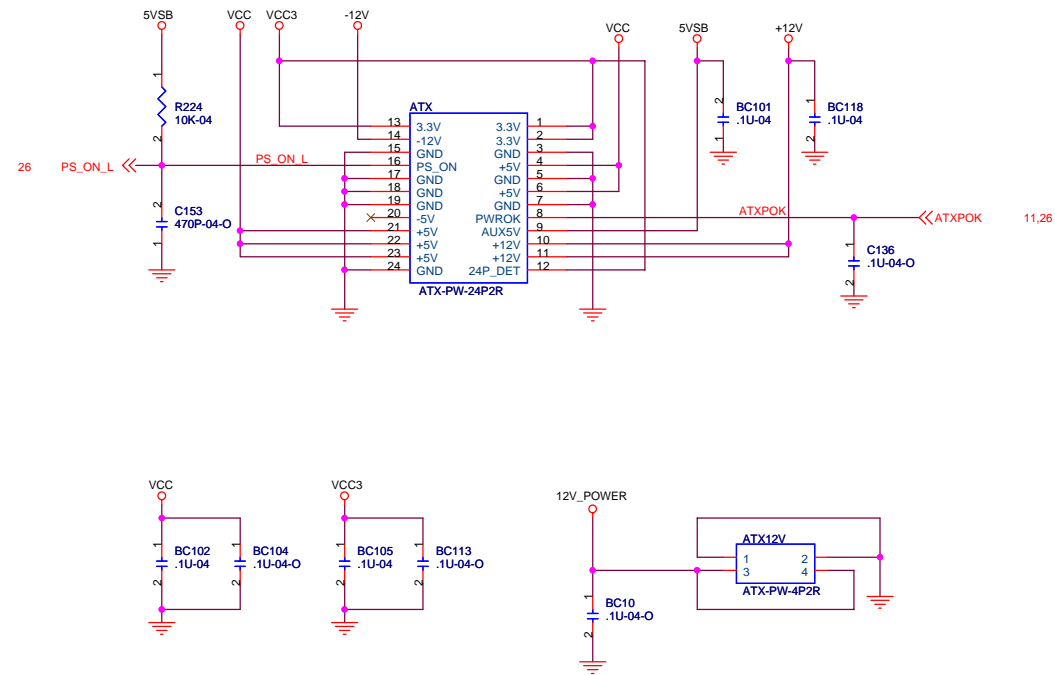
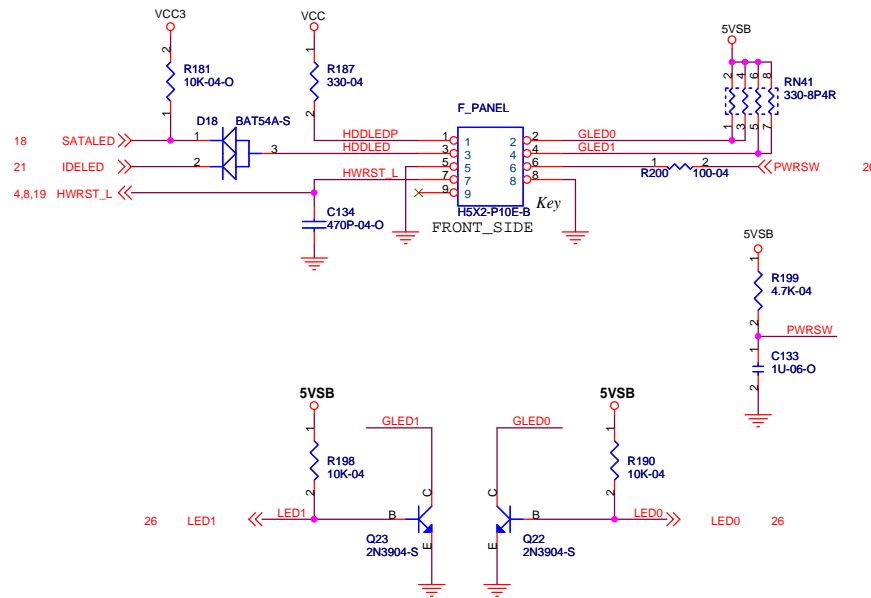
* Placement : Put that CAPs x2 on solder side

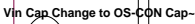


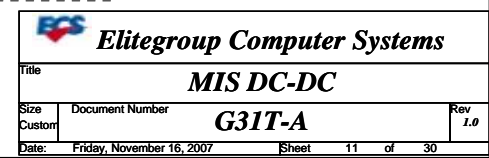
1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

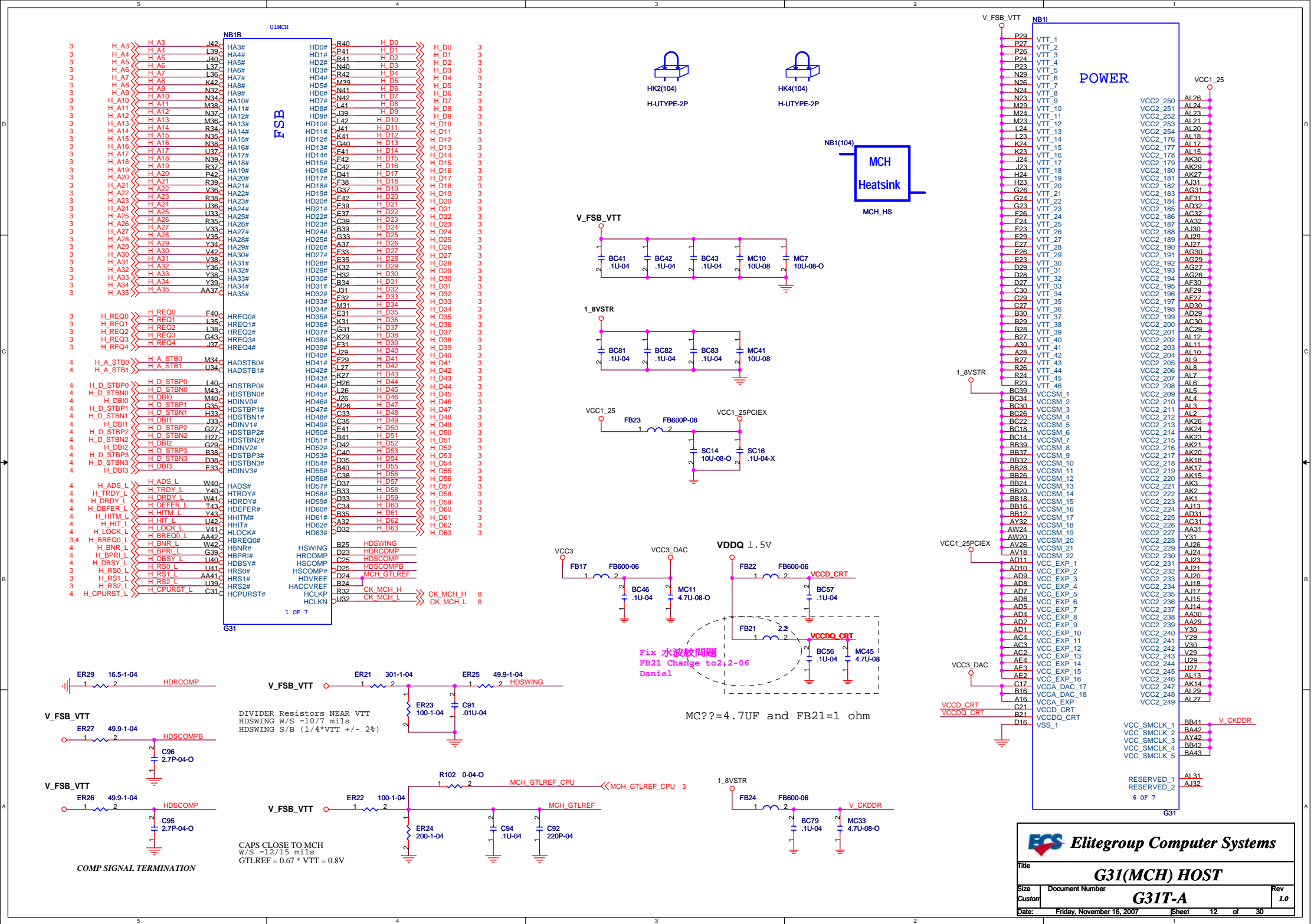


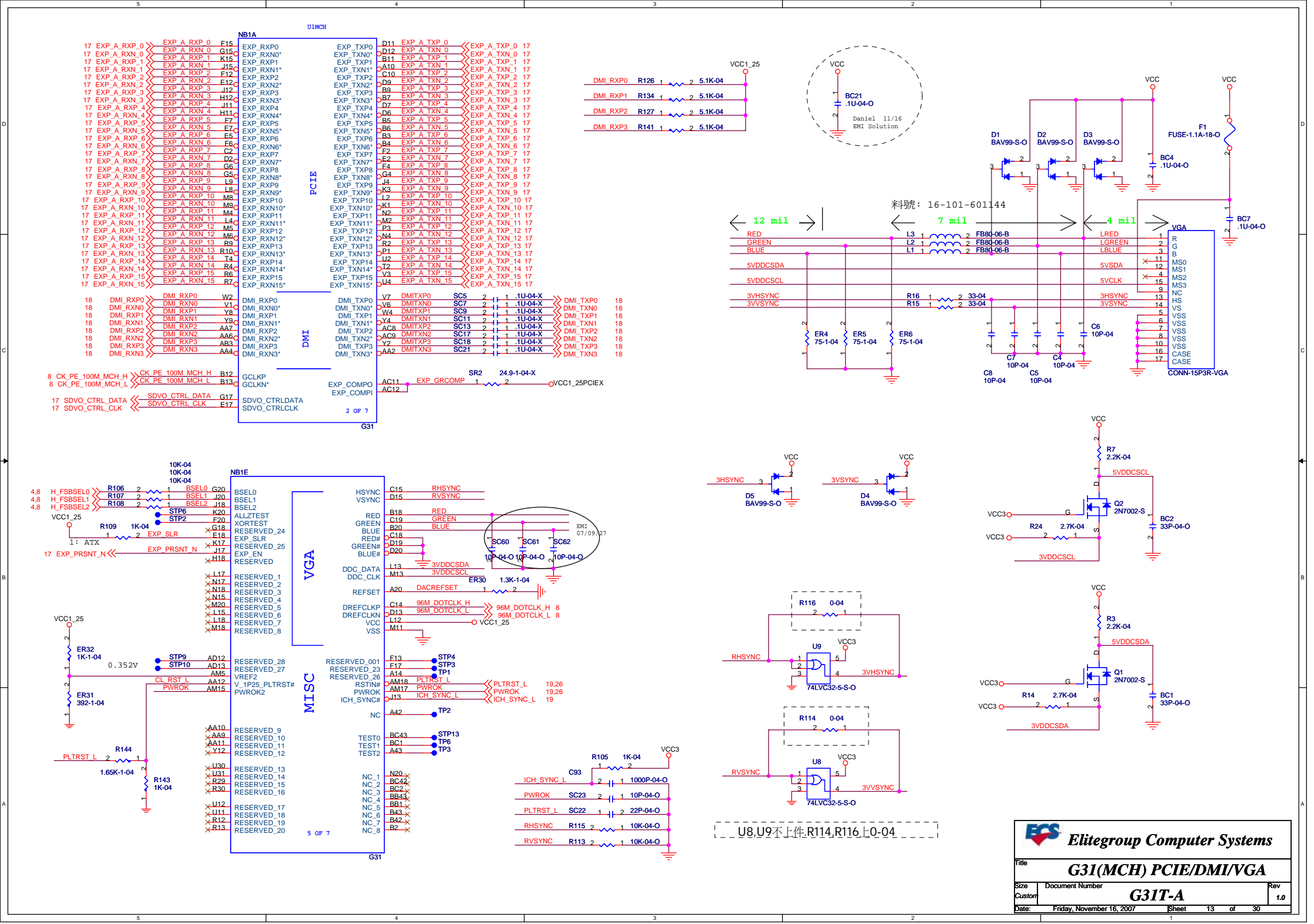
BSEL TABLE
2 1 0 PSB FREQUENCY
0 0 1 133 MHZ (533)
0 1 0 200 MHZ (800)

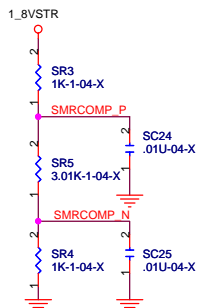
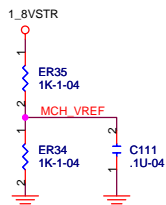




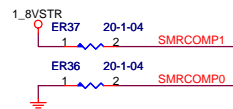
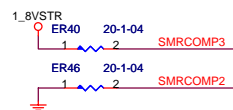








DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_SM INTERNAL
BUFFERS SET TO 20 OHMS



NB1C		U1MCH	
MAAA_0	BA31	SMA_A0	SDQS_A0
MAAA_1	BA25	SMA_A1	SDQS_A0#
MAAA_2	BA26	SMA_A2	SDM_A0
MAAA_3	BA25	SMA_A3	
MAAA_4	AY25	SMA_A4	SDQ_A0
MAAA_5	BA23	SMA_A5	SDQ_A1
MAAA_6	AY24	SMA_A6	SDQ_A2
MAAA_7	AY23	SMA_A7	SDQ_A3
MAAA_8	BB23	SMA_A8	SDQ_A4
MAAA_9	BA22	SMA_A9	SDQ_A5
MAAA_10	AY33	SMA_A10	SDQ_A6
MAAA_11	BB22	SMA_A11	SDQ_A7
MAAA_12	AW21	SMA_A12	
MAAA_13	AY38	SMA_A13	SDQS_A1
MAAA_14	BA21	SMA_A14	SDQS_A1#
SWE_L_A	BB34	SWE_A#	SDM_A1
SCAS_L_A	AY35	SCAS_A#	SDQ_A8
SRAS_L_A	BB35	SRAS_A#	SDQ_A9
SBSA_0	BA33	SBS_A0	SDQ_A10
SBSA_1	AW32	SBS_A1	SDQ_A11
SBSA_2	BB21	SBS_A2	SDQ_A12
CSA_L0	AW35	SCS_A0#	SDQ_A13
CSA_L1	BA35	SCS_A1#	SDQ_A14
	BA34	RESERVED_11	SDQ_A15
	BB38	RESERVED_12	
CKEA_0	BC20	SCKE_A0	SDQS_A2
CKEA_1	AY20	SCKE_A1	SDQS_A2#
	AY21	RESERVED_9	SDM_A2
	BA19	RESERVED_10	
ODTA_0	AY37	SODT_A0	SDQ_A16
ODTA_1	BA38	SODT_A1	SDQ_A17
	BB35	RESERVED_2	SDQ_A18
	BA39	RESERVED_1	SDQ_A19
DCLKA_H0	AU31	SCLK_A0	SDQ_A20
DCLKA_L0	AR31	SCLK_A0#	SDQ_A21
DCLKA_H1	AP27	SCLK_A1	SDQ_A22
DCLKA_L1	AN27	SCLK_A1#	SDQ_A23
DCLKA_H2	AV33	SCLK_A2	
DCLKA_L2	AW33	SCLK_A2#	SDQ_A24
	AP29	RESERVED_3	SDQ_A25
	AP31	RESERVED_4	SDQ_A26
	AM26	RESERVED_5	SDQ_A27
	AM27	RESERVED_6	SDQ_A28
	AT33	RESERVED_7	SDQ_A29
	AU33	RESERVED_8	SDQ_A30
			SDQ_A31
SDQS_A4		AR41	DQS_H_A4
SDQS_A4#		AR40	DQS_L_A4
SDM_A4		AU43	MPD_A4
		AV42	MD_A32
		AU40	MD_A33
		AP42	MD_A34
		AN39	MD_A35
		AV40	MD_A36
		AG34	MD_A37
		AP41	MD_A38
		AP41	MD_A39
SDQS_A5		AL41	DQS_H_A5
SDQS_A5#		AL40	DQS_L_A5
SDM_A5		AM43	MPD_A5
		AN41	MD_A40
		AM39	MD_A41
		AK42	MD_A42
		AK41	MD_A43
		AN40	MD_A44
		AN42	MD_A45
		AL42	MD_A46
		AL39	MD_A47
SDQS_A6		AG42	DQS_H_A6
SDQS_A6#		AG41	DQS_L_A6
SDM_A6		AG40	MPD_A6
		AJ40	MD_A48
		AH43	MD_A49
		AE39	MD_A50
		AE40	MD_A51
		AJ42	MD_A52
		AJ41	MD_A53
		AF41	MD_A54
		AF42	MD_A55
SDQS_A7		AC42	DQS_H_A7
SDQS_A7#		AC41	DQS_L_A7
SDM_A7		AC40	MPD_A7
		AD40	MD_A56
		AD43	MD_A57
		AB41	MD_A58
		AA40	MD_A59
		AE42	MD_A60
		AE41	MD_A61
		AC39	MD_A62
		AB42	MD_A63

DDR_0

AN21

RESERVED

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G31

NB1D		U1MCH	
MAAB_0	BB17	SMA_B0	SDQS_B0
MAAB_1	AY17	SMA_B1	SDQS_B0#
MAAB_2	BA17	SMA_B2	SDM_B0
MAAB_3	BC16	SMA_B3	
MAAB_4	AW15	SMA_B4	SDQ_B0
MAAB_5	BA15	SMA_B5	SDQ_B1
MAAB_6	BB15	SMA_B6	SDQ_B2
MAAB_7	BA14	SMA_B7	SDQ_B3
MAAB_8	AY15	SMA_B8	SDQ_B4
MAAB_9	BB14	SMA_B9	SDQ_B5
MAAB_10	AW18	SMA_B10	SDQ_B6
MAAB_11	BB13	SMA_B11	SDQ_B7
MAAB_12	BA13	SMA_B12	
MAAB_13	AY29	SMA_B13	SDQS_B1
MAAB_14	AY13	SMA_B14	SDQS_B1#
SWE_L_B	BA27	SWE_B#	SDM_B1
SCAS_L_B	AW29	SCAS_B#	SDQ_B8
SRAS_L_B	AW26	SRAS_B#	SDQ_B9
SBSB_0	AY19	SBS_B0	SDQ_B10
SBSB_1	BA18	SBS_B1	SDQ_B11
SBSB_2	BC12	SBS_B2	SDQ_B12
CSB_L0	BB27	SCS_B0#	SDQ_B13
CSB_L1	BB30	SCS_B1#	SDQ_B14
	AY27	RESERVED_13	SDQ_B15
	AY31	RESERVED_10	
CKEB_0	AY12	SCKE_B0	SDQS_B2
CKEB_1	AW12	SCKE_B1	SDQS_B2#
	BB11	RESERVED_11	SDM_B2
	BA11	RESERVED_12	
ODTB_0	BA29	SODT_B0	SDQ_B16
ODTB_1	BA30	SODT_B1	SDQ_B17
	BB29	RESERVED_14	SDQ_B18
	BB31	RESERVED_15	SDQ_B19
DCLKB_H0	AV31	SCLK_B0	SDQ_B20
DCLKB_H1	AW32	SCLK_B0#	SDQ_B21
DCLKB_L1	AT27	SCLK_B1	SDQ_B22
DCLKB_H2	AV32	SCLK_B1#	SDQ_B23
DCLKB_L2	AT32	SCLK_B2	
	AU29	SCLK_B2#	SDQ_B24
	AR29	RESERVED_16	SDQ_B25
	AV29	RESERVED_17	SDQ_B26
	AW27	RESERVED_18	SDQ_B27
	AN33	RESERVED_19	SDQ_B28
	AP32	RESERVED_20	SDQ_B29
		RESERVED_21	SDQ_B30
			SDQ_B31
SDQS_B4		AW39	DQS_H_B4
SDQS_B4#		AU39	DQS_L_B4
SDM_B4		AU37	MPD_B4
		AV37	MD_B32
		AV38	MD_B33
		AN36	MD_B34
		AN35	MD_B35
		AN37	MD_B36
		AN35	MD_B37
		AN35	MD_B38
		AN37	MD_B39
SDQS_B5		AL35	DQS_H_B5
SDQS_B5#		AL34	DQS_L_B5
SDM_B5		AM37	MPD_B5
		AM35	MD_B40
		AM38	MD_B41
		AJ34	MD_B42
		AL38	MD_B43
		AR39	MD_B44
		AM34	MD_B45
		AL37	MD_B46
		AL32	MD_B47
SDQS_B6		AG35	DQS_H_B6
SDQS_B6#		AG36	DQS_L_B6
SDM_B6		AG39	MPD_B6
		AG38	MD_B48
		AJ38	MD_B49
		AF36	MD_B50
		AF33	MD_B51
		AJ37	MD_B52
		AJ35	MD_B53
		AG33	MD_B54
		AF34	MD_B55
SDQS_B7		AC36	DQS_H_B7
SDQS_B7#		AC37	DQS_L_B7
SDM_B7		AD38	MPD_B7
		AD36	MD_B56
		AC33	MD_B57
		AA34	MD_B58
		AA36	MD_B59
		AD34	MD_B60
		AF38	MD_B61
		AC34	MD_B62
		AA33	MD_B63

DDR_1

AM21

MCH VREF

SVREF

SMRCOMP0

SMRCOMP1

SMRCOMP2

SMRCOMP3

SMRCOMP N

SMRCOMP P

SMRCOMPVOL

SMRCOMPVOH

RESERVED

AN2

AN3

BB40

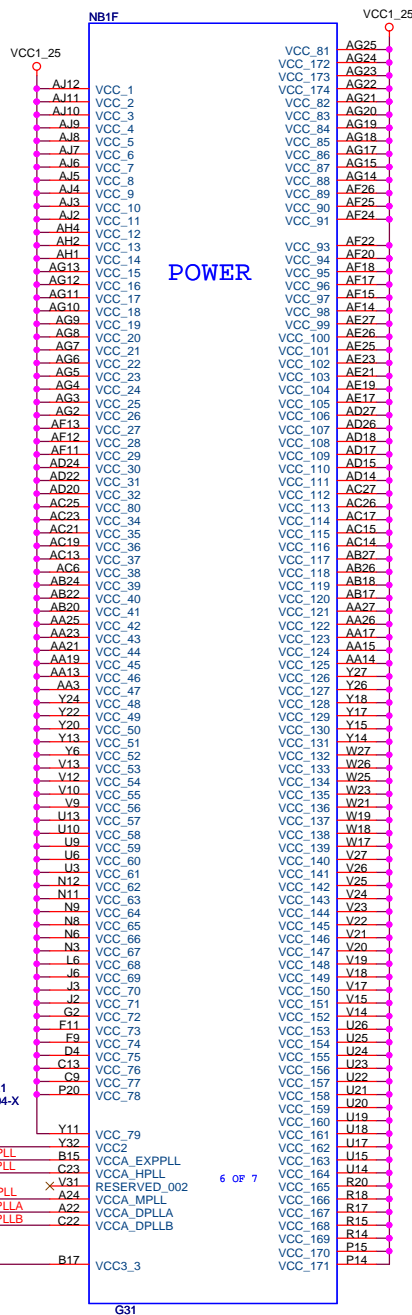
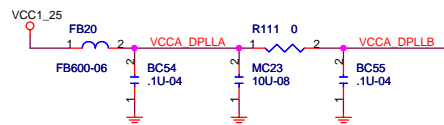
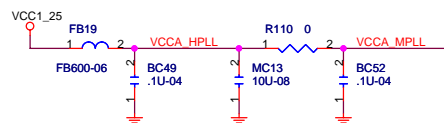
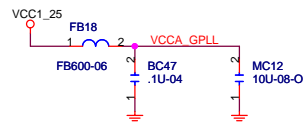
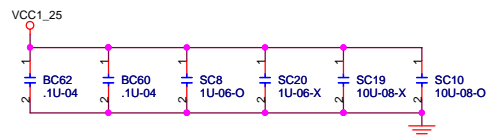
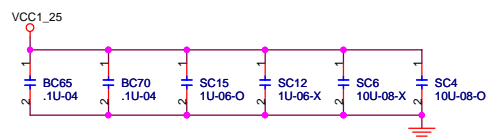
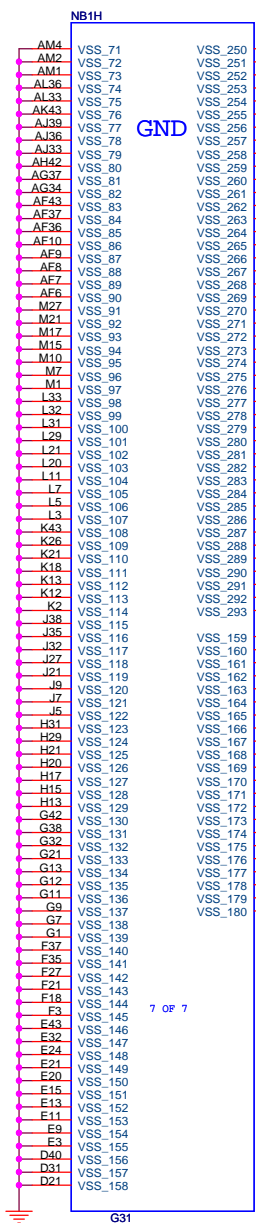
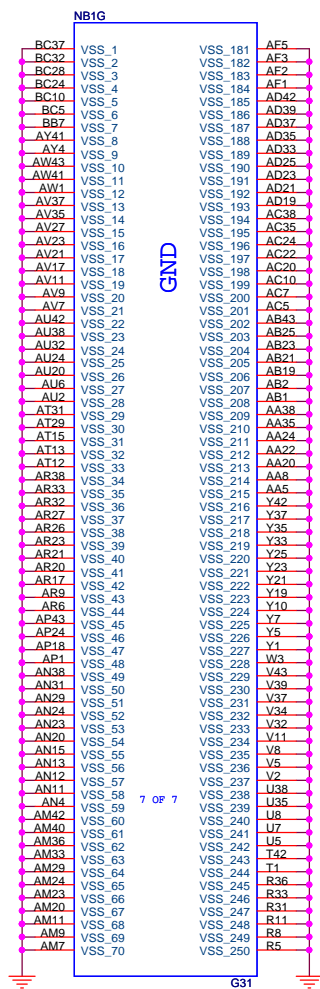
BA40

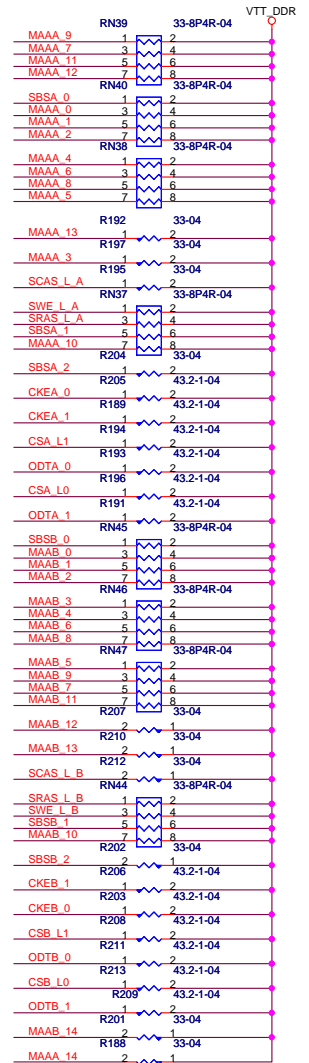
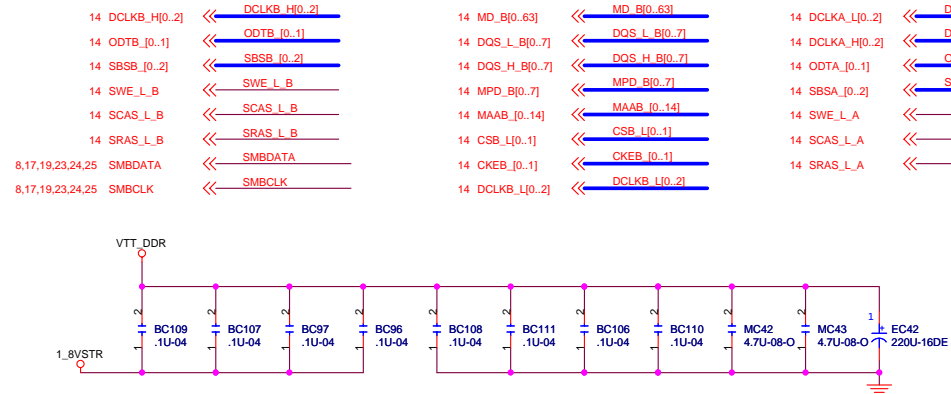
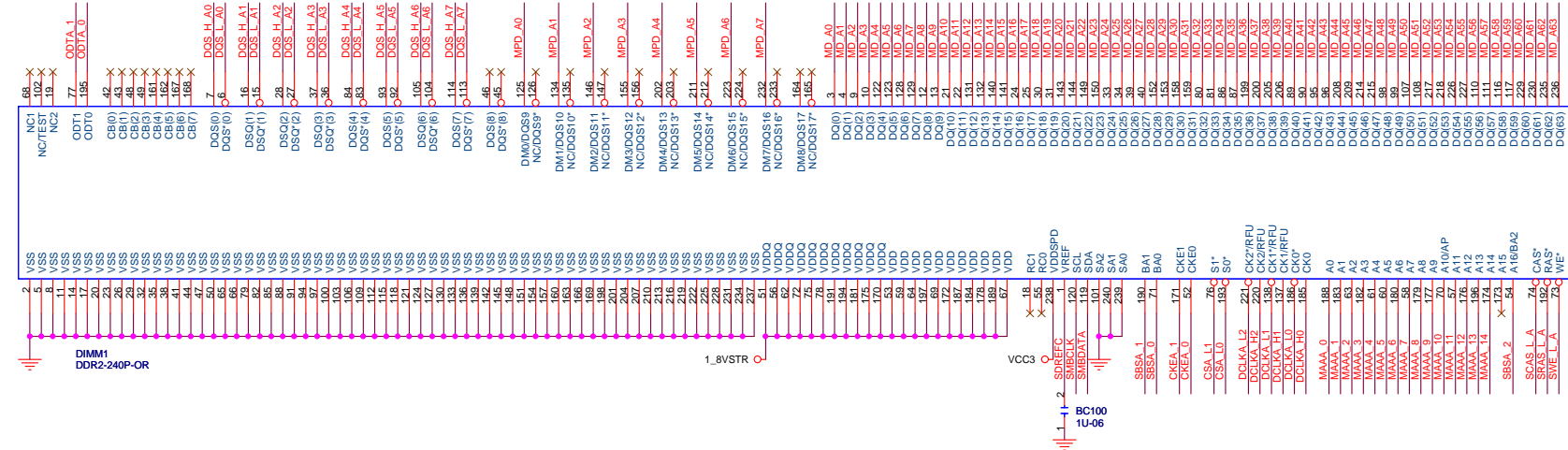
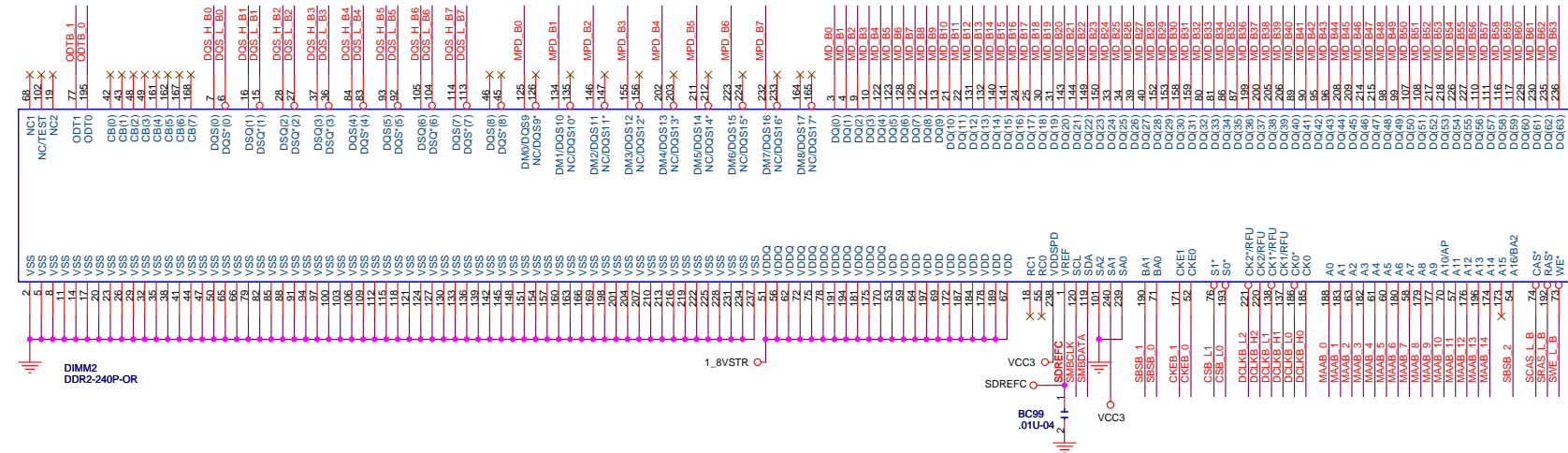
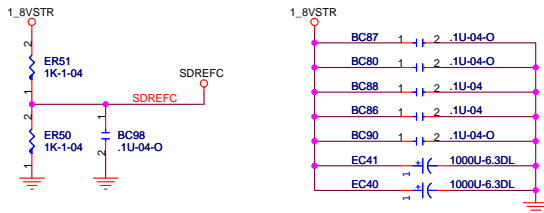
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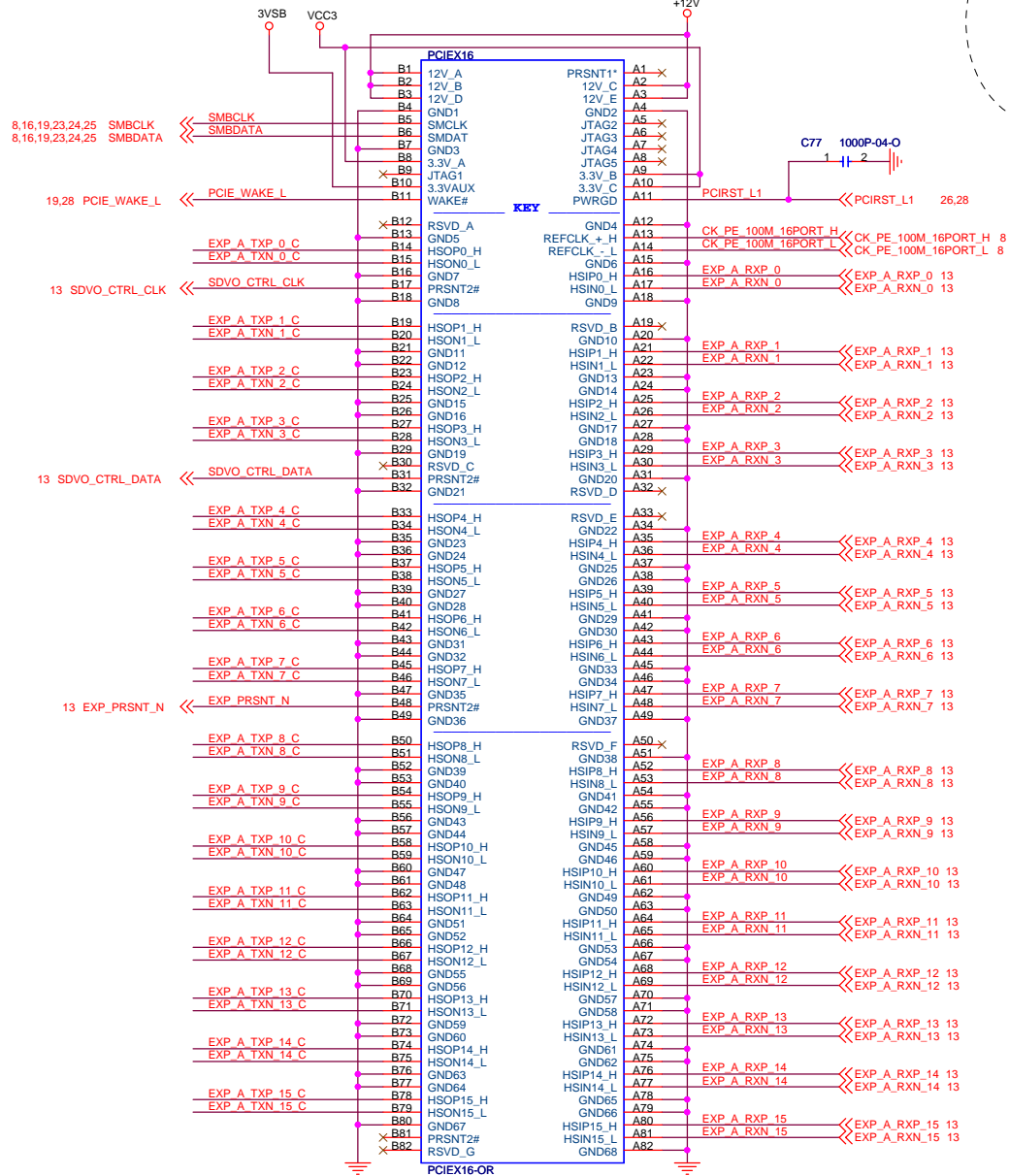
BB19

4 OF 7

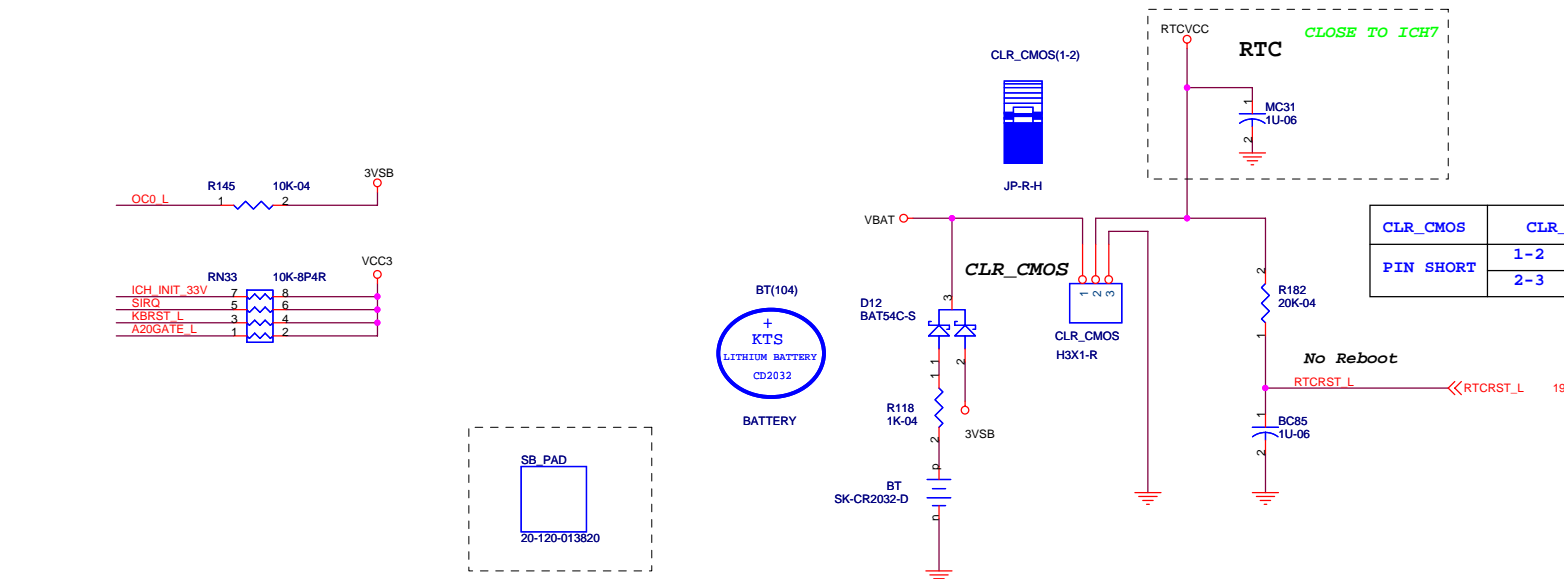
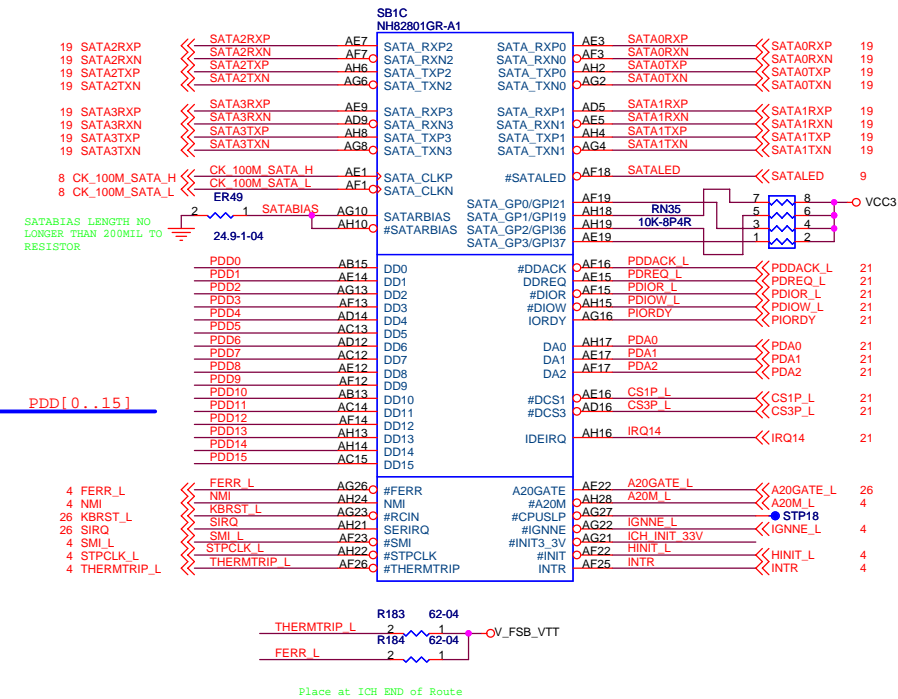
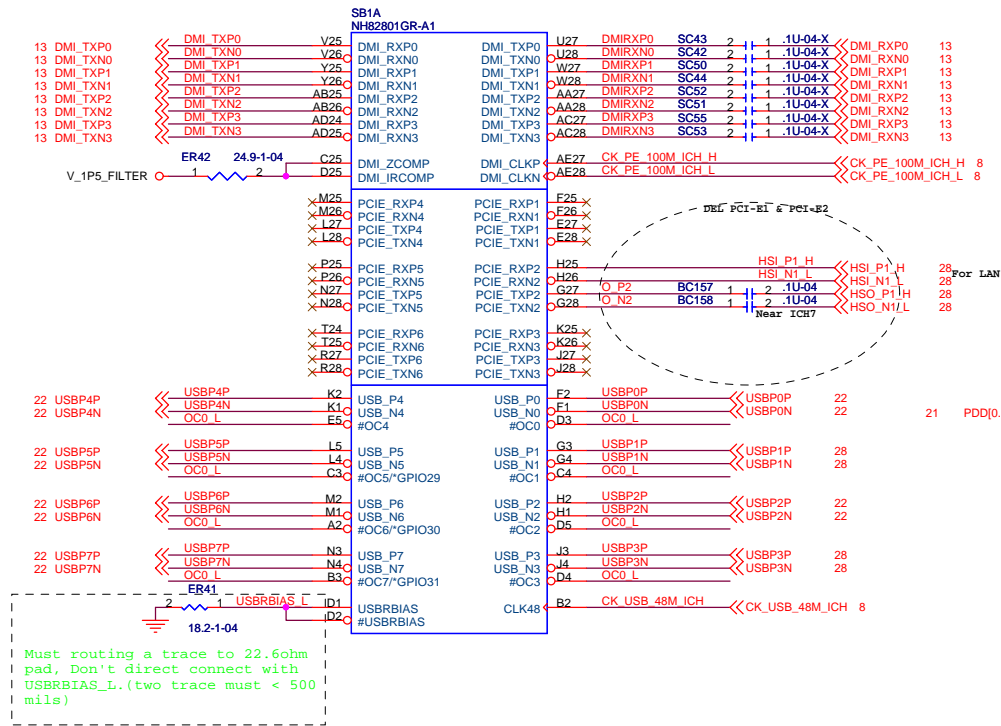
G31

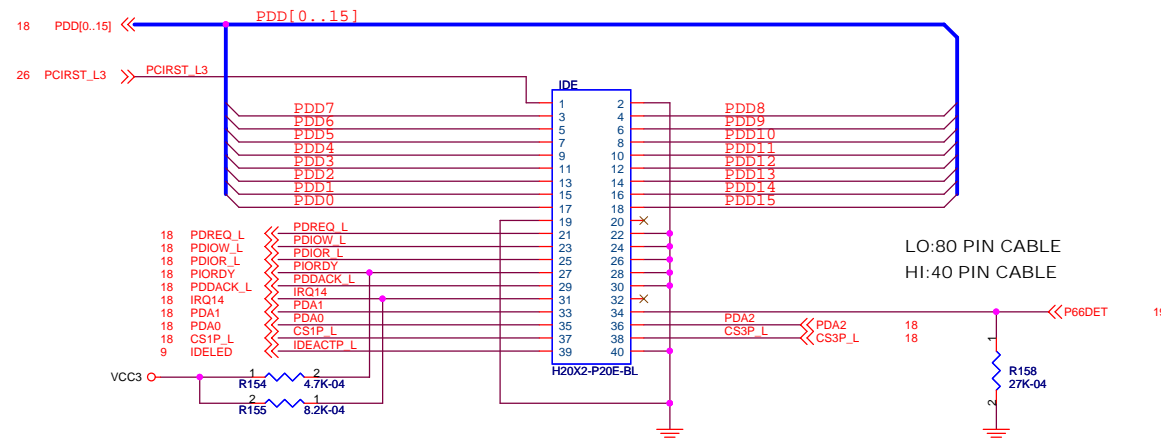




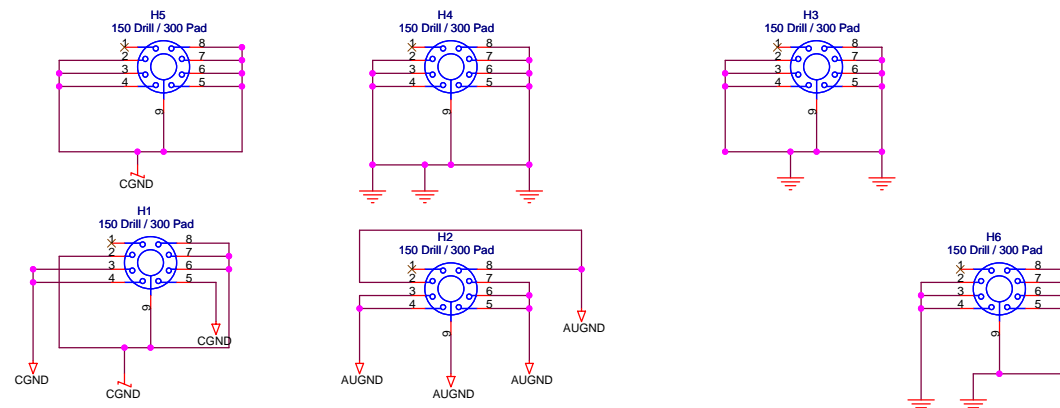


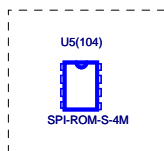
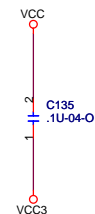
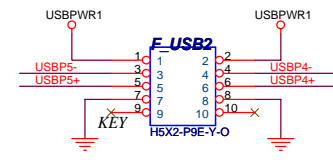
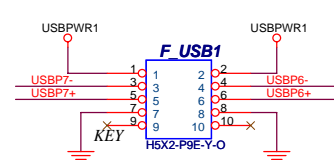
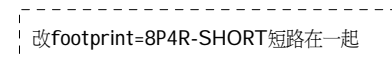
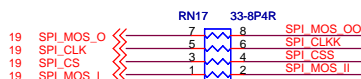
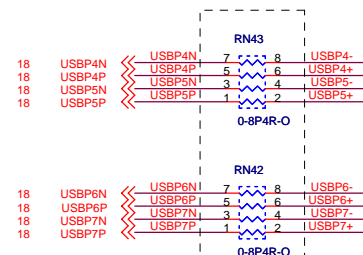
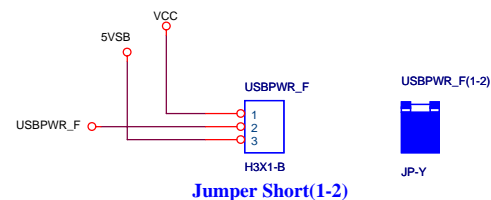
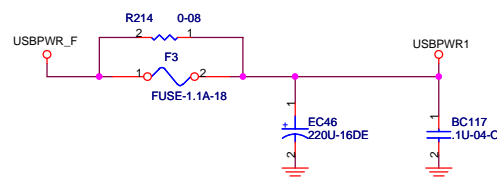
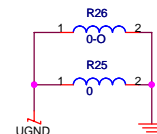
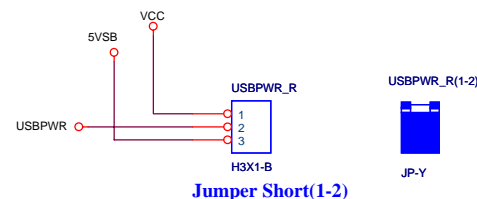
EXP_A_TXP_0_C	BC28	1	2	.1U-04	EXP_A_TXP_0	EXP_A_TXP_0_13
EXP_A_TXN_0_C	BC27	1	2	.1U-04	EXP_A_TXN_0	EXP_A_TXN_0_13
EXP_A_TXP_1_C	BC31	1	2	.1U-04	EXP_A_TXP_1	EXP_A_TXP_1_13
EXP_A_TXN_1_C	BC32	1	2	.1U-04	EXP_A_TXN_1	EXP_A_TXN_1_13
EXP_A_TXP_2_C	BC33	1	2	.1U-04	EXP_A_TXP_2	EXP_A_TXP_2_13
EXP_A_TXN_2_C	BC34	1	2	.1U-04	EXP_A_TXN_2	EXP_A_TXN_2_13
EXP_A_TXP_3_C	BC35	1	2	.1U-04	EXP_A_TXP_3	EXP_A_TXP_3_13
EXP_A_TXN_3_C	BC37	1	2	.1U-04	EXP_A_TXN_3	EXP_A_TXN_3_13
EXP_A_TXP_4_C	BC38	1	2	.1U-04	EXP_A_TXP_4	EXP_A_TXP_4_13
EXP_A_TXN_4_C	BC39	1	2	.1U-04	EXP_A_TXN_4	EXP_A_TXN_4_13
EXP_A_TXP_5_C	BC44	1	2	.1U-04	EXP_A_TXP_5	EXP_A_TXP_5_13
EXP_A_TXN_5_C	BC40	1	2	.1U-04	EXP_A_TXN_5	EXP_A_TXN_5_13
EXP_A_TXP_6_C	BC48	1	2	.1U-04	EXP_A_TXP_6	EXP_A_TXP_6_13
EXP_A_TXN_6_C	BC45	1	2	.1U-04	EXP_A_TXN_6	EXP_A_TXN_6_13
EXP_A_TXP_7_C	BC51	1	2	.1U-04	EXP_A_TXP_7	EXP_A_TXP_7_13
EXP_A_TXN_7_C	BC50	1	2	.1U-04	EXP_A_TXN_7	EXP_A_TXN_7_13
EXP_A_TXP_8_C	BC53	1	2	.1U-04	EXP_A_TXP_8	EXP_A_TXP_8_13
EXP_A_TXN_8_C	BC58	1	2	.1U-04	EXP_A_TXN_8	EXP_A_TXN_8_13
EXP_A_TXP_9_C	BC59	1	2	.1U-04	EXP_A_TXP_9	EXP_A_TXP_9_13
EXP_A_TXN_9_C	BC61	1	2	.1U-04	EXP_A_TXN_9	EXP_A_TXN_9_13
EXP_A_TXP_10_C	BC64	1	2	.1U-04	EXP_A_TXP_10	EXP_A_TXP_10_13
EXP_A_TXN_10_C	BC63	1	2	.1U-04	EXP_A_TXN_10	EXP_A_TXN_10_13
EXP_A_TXP_11_C	BC67	1	2	.1U-04	EXP_A_TXP_11	EXP_A_TXP_11_13
EXP_A_TXN_11_C	BC66	1	2	.1U-04	EXP_A_TXN_11	EXP_A_TXN_11_13
EXP_A_TXP_12_C	BC69	1	2	.1U-04	EXP_A_TXP_12	EXP_A_TXP_12_13
EXP_A_TXN_12_C	BC68	1	2	.1U-04	EXP_A_TXN_12	EXP_A_TXN_12_13
EXP_A_TXP_13_C	BC73	1	2	.1U-04	EXP_A_TXP_13	EXP_A_TXP_13_13
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EXP_A_TXP_14_C	BC75	1	2	.1U-04	EXP_A_TXP_14	EXP_A_TXP_14_13
EXP_A_TXN_14_C	BC74	1	2	.1U-04	EXP_A_TXN_14	EXP_A_TXN_14_13
EXP_A_TXP_15_C	BC78	1	2	.1U-04	EXP_A_TXP_15	EXP_A_TXP_15_13
EXP_A_TXN_15_C	BC77	1	2	.1U-04	EXP_A_TXN_15	EXP_A_TXN_15_13



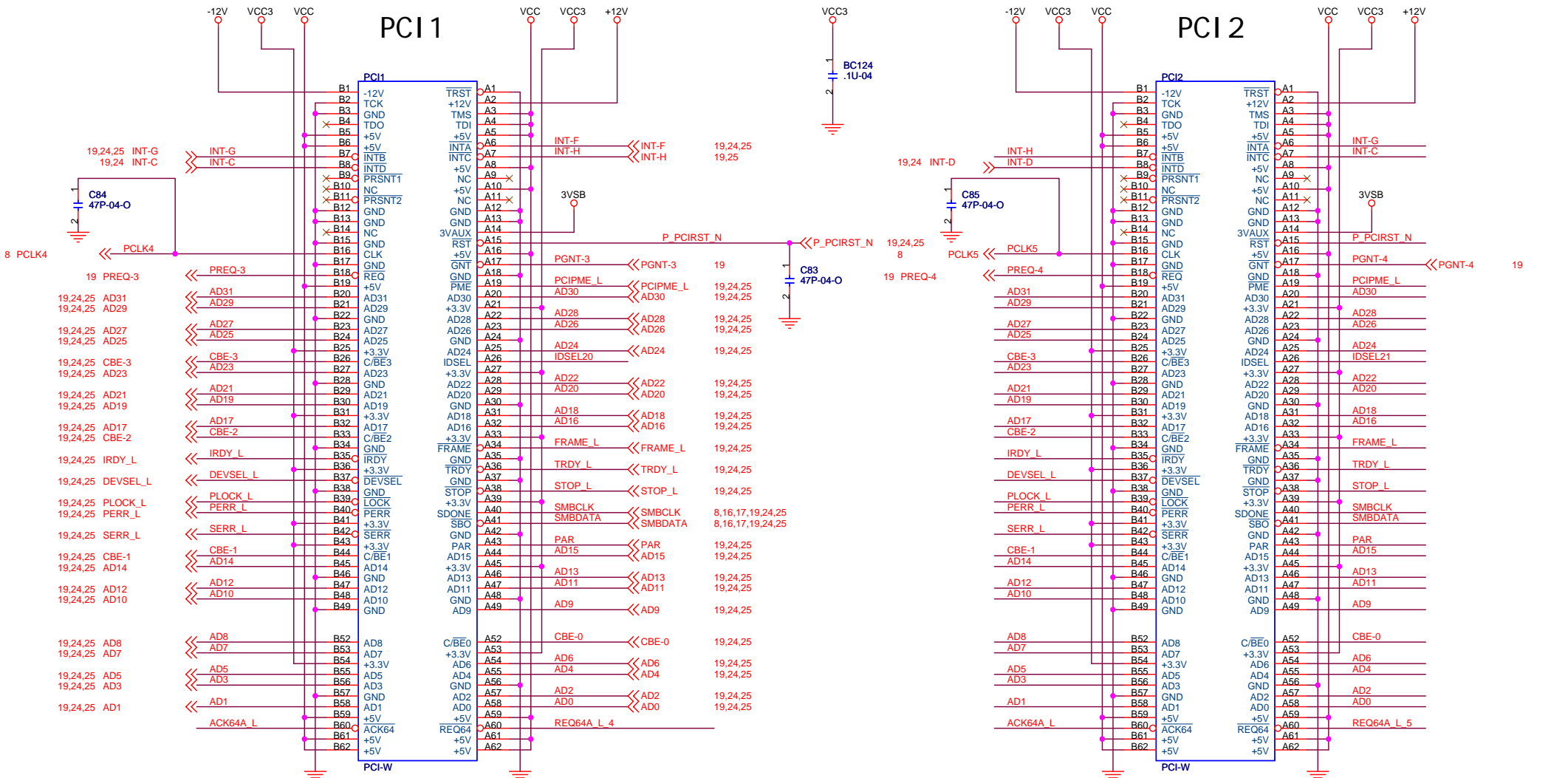


DATA LINES SHOULD BE MATCHED TO STROBES (PDIOR_L , PIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



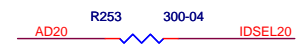


8 ROM(量產時不含SOCKET)



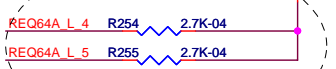
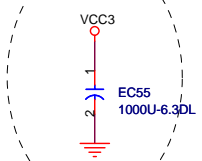
PCI1-INT:
INTA: INTF
INTB: INTG
INTC: INTH
INTD: INTI

IDSEL=AD20
REQ=PREQ3#
GNT=PGNT3#



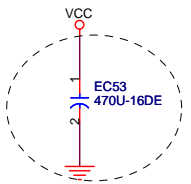
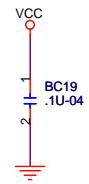
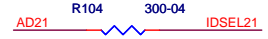
07/06/08 ADD
Daniel

ADD EC47 FOR VCC3
Daniel 07/09/06



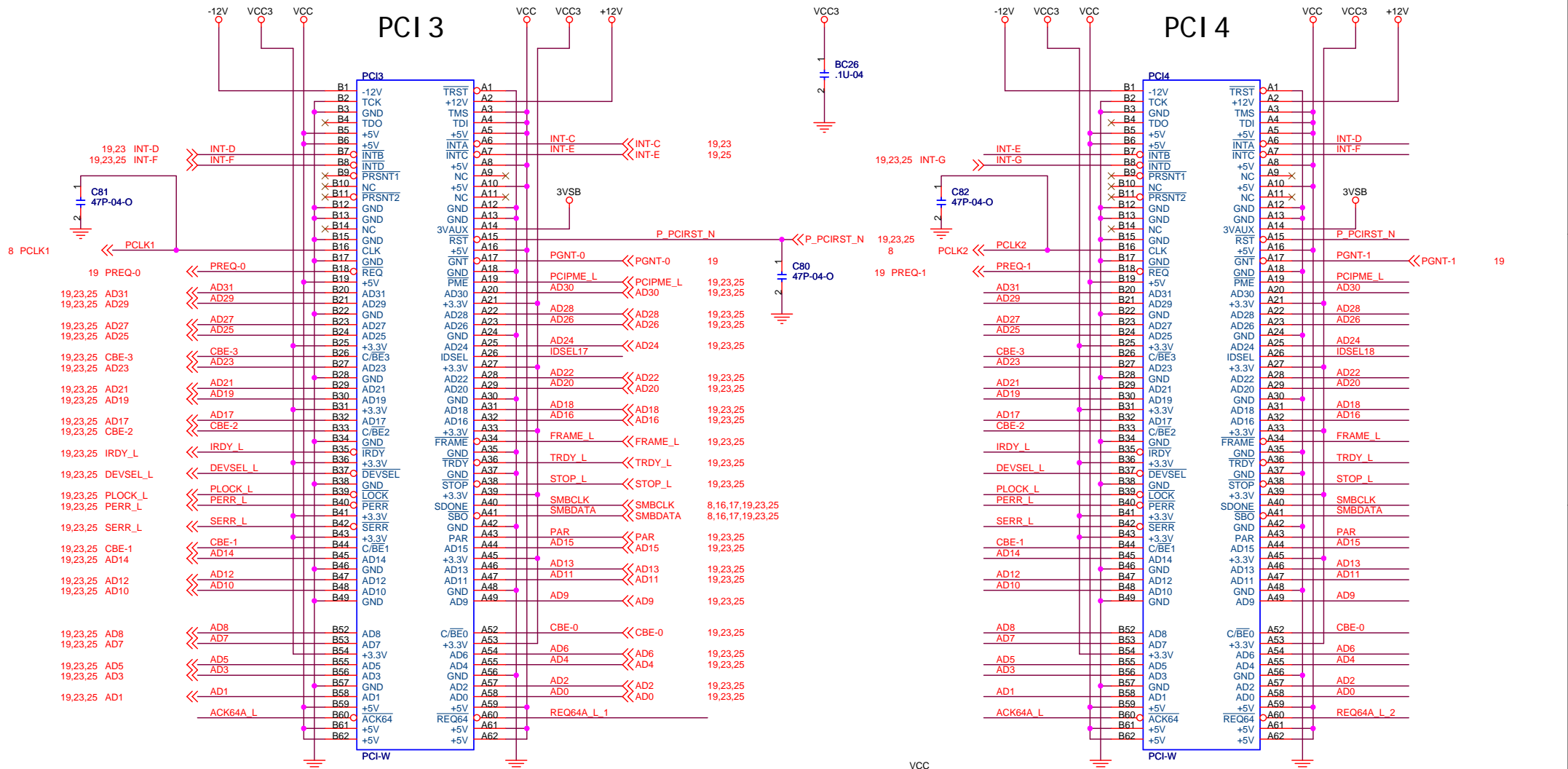
PCI2-INT:
INTA: INTG
INTB: INTH
INTC: INTI
INTD: INTJ

IDSEL=AD21
REQ=PREQ4#
GNT=PGNT4#



PCI 3

PCI 4



PCI1-INT:
INTA:INTC
INTB:INTD
INTC:INTE
INTD:INTF

IDSEL=AD17
REQ=PREQ0#
GNT=PGNT0#

AD17 R99 300-04 IDSEL17

ACK64A_L << ACK64A_L 23,25

07/06/08 ADD
Dapig1

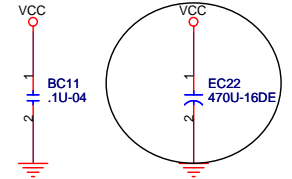
STOP_L RN15 2 1 2.7K-8P4R
PLOCK_L 4 3 3
PERR_L 6 5 5
SERR_L 8 7 7
FRAME_L RN14 2 1 2.7K-8P4R
IRDY_L 4 3 3
TRDY_L 6 5 5
DEVSEL_L 8 7 7
REQ64A_L 1 RN16 2 1 2.7K-8P4R
ACK64A_L 4 3 3
REQ64A_L 2 6 5
PAR 8 7 7

INT-F RN10 1 2 8.2K-8P4R
INT-E 3 4 4
INT-C 5 6 6
INT-D 7 8 8

PCI2-INT:
INTA:INTD
INTB:INTE
INTC:INTF
INTD:INTG

IDSEL=AD18
REQ=PREQ1#
GNT=PGNT1#

AD18 R100 300-04 IDSEL18



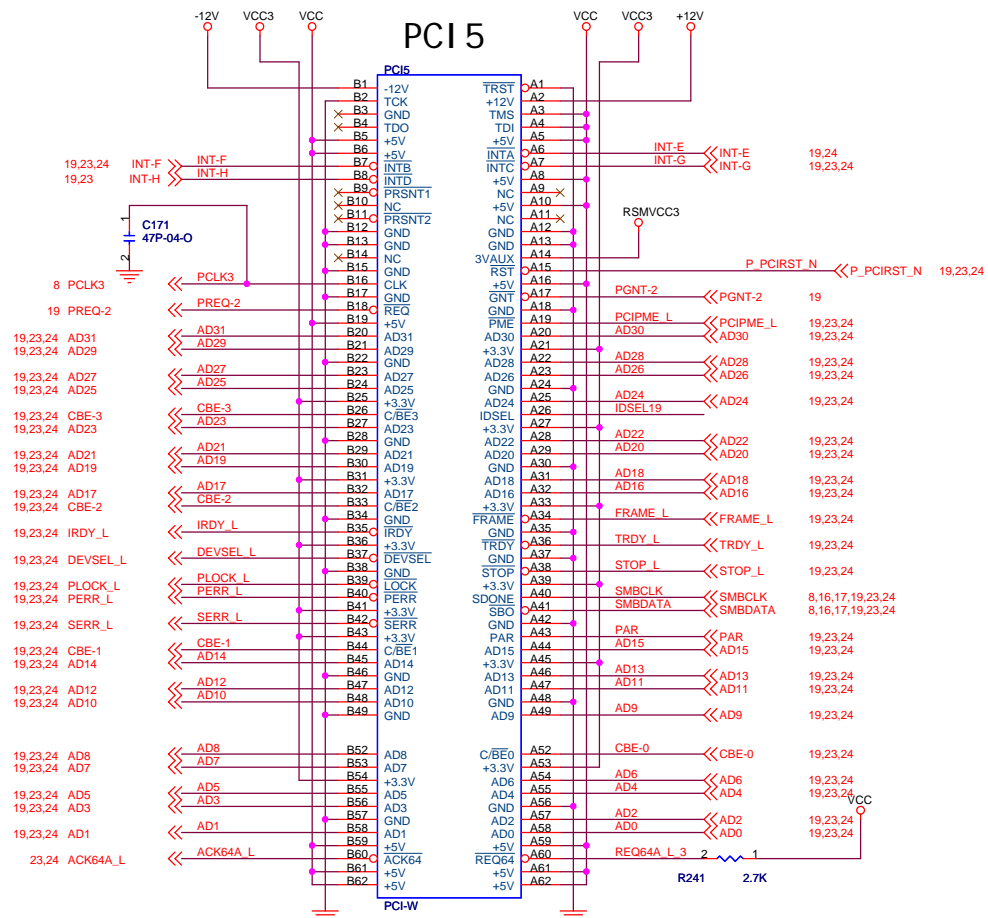
Elitegroup Computer Systems

Title
Size Custom Document Number
Date: Friday, November 16, 2007 Sheet 24 of 30

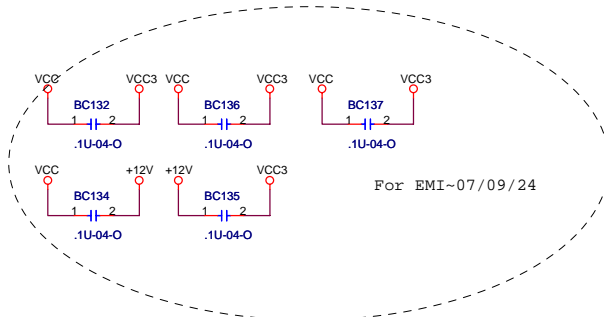
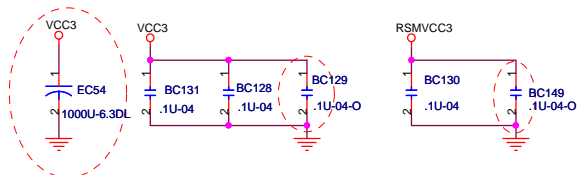
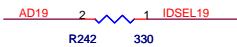
PCI Slot 3&4

G31T-A

Rev 1.0



PCI3-INT#: IDSEL=AD19
 INTA: INT# REQ=PREQ2#
 INTB: INT# GNT=PGNT2#
 INT# : INT#
 INTD: INT#



修改U3 Value:8718F



add LPT Net
07/09/17
Daniel

增加BC126靠近BC8

增加BC122,BC123靠近PSKBM

PS2-KB-MS改成無彈片

THERM. SENSING

install PECI when 8718

Close to Place the Pin67

Close to Place the Pin99

IOGND have to 10mil width

R69改不上件,BC13改成3300P-04

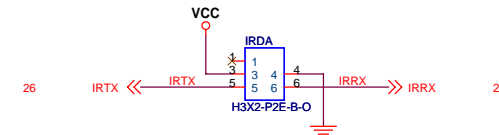
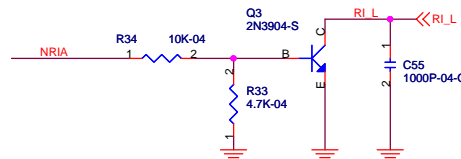
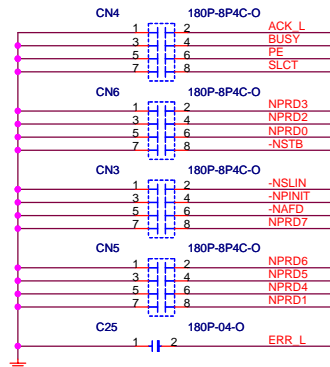
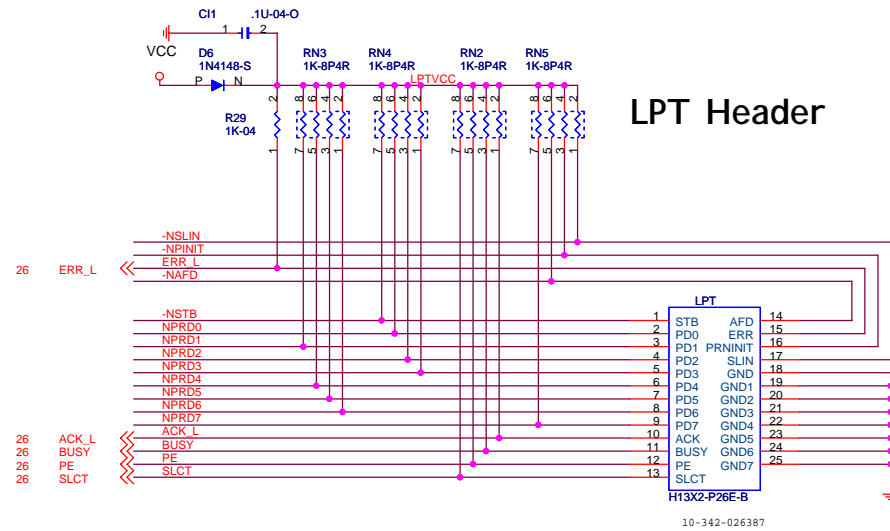
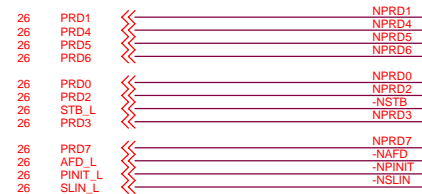
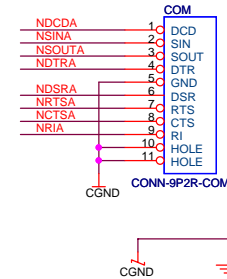
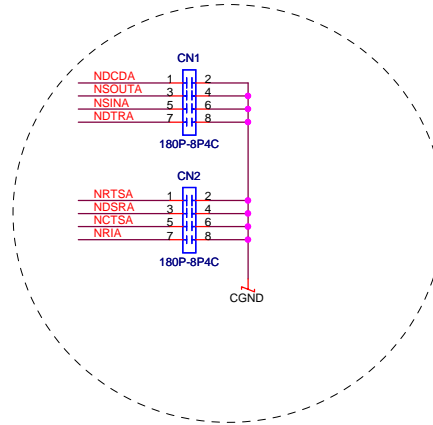
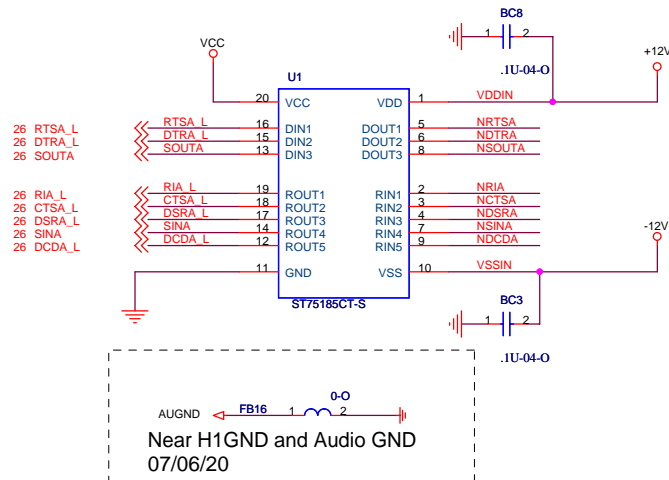


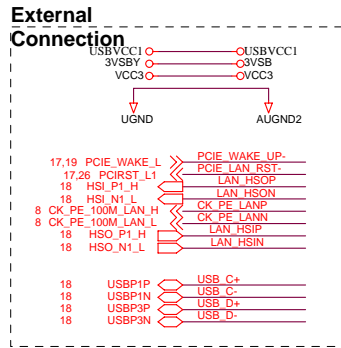
Elitegroup Computer Systems

LPC_FDD/KB/M

G31T-A

Title		Rev	
Size		1.0	
Document Number		G31T-A	
Date		Friday, November 16, 2007	
Sheet		26 of 30	





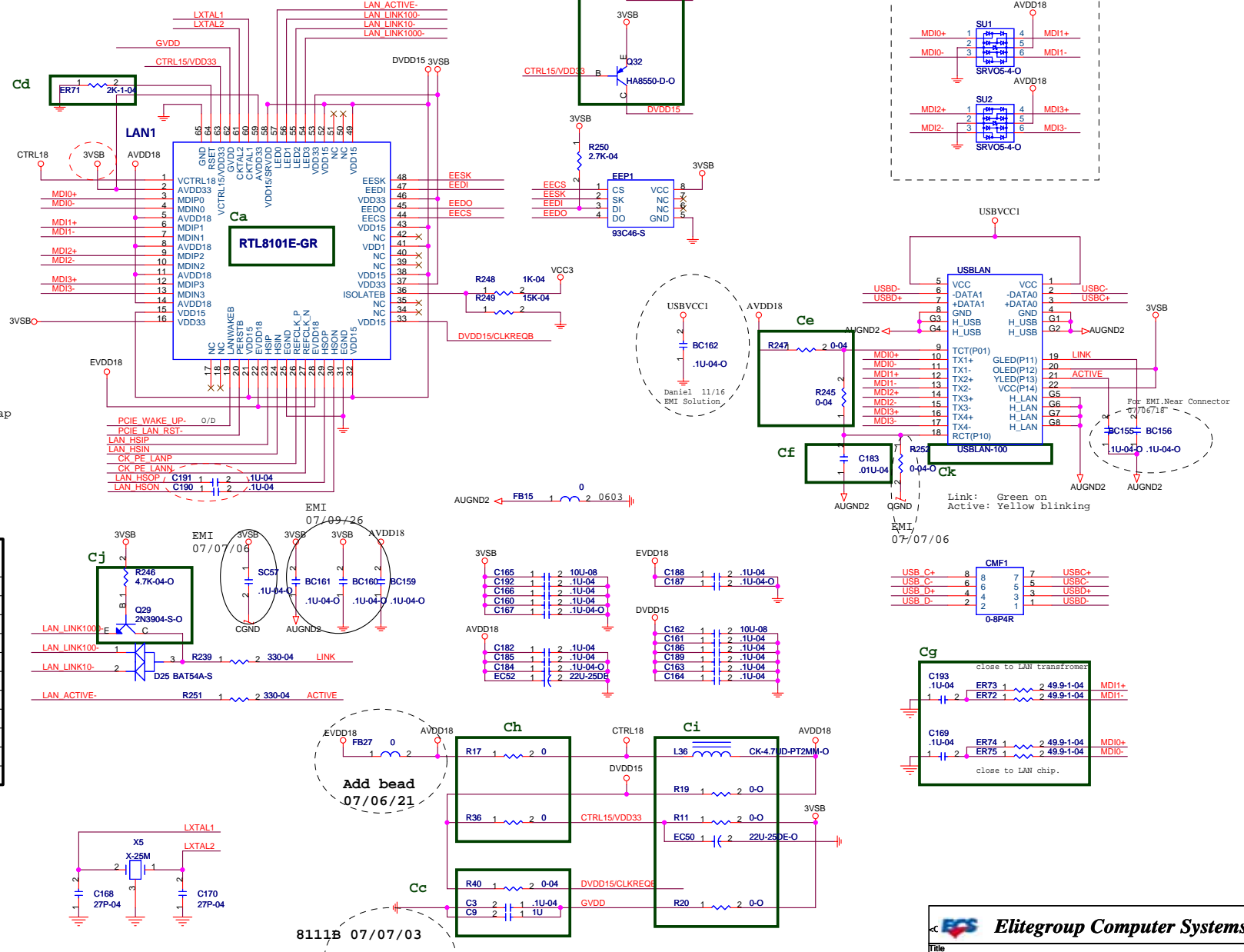
新手提醒:
 LAN_HSOP/N請接到SB的PCIE RX端
 LAN_HSIP/N請接到SB的PCIE TX端
 LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

BOM Difference

	RTL8101E-GR 10/100M	RTL8111C-GR 1000M	RTL8111B-GR 1000M
Ca	RTL8101E-GR	RTL8111C-GR	RTL8111B-GR
Cb	X	X	V
Cc	V	X	V
Cd	2K-1-04	2.49K-1-04	2.49K-1-04
Ce	V	X	X
Cf	.01U-04	0-04	0-04
Cg	V	X	X
Ch	V	X	X
Ci	X	V	X
Cj	X	V	V
Ck	USBLAN-100	USBLAN-1000	USBLAN-1000

Power Difference

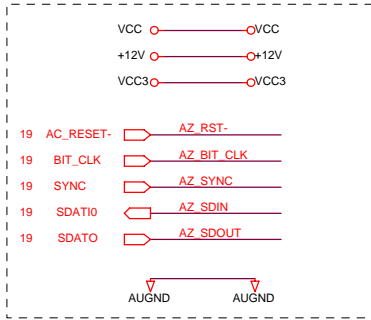
	RTL8101E	RTL8111C	RTL8111B
AVDD33	3.3V	3.3V	3.3V
AVDD18	1.8V	1.2V	1.8V
EVDD18	1.8V	1.2V	1.8V
DVDD15	1.5V	1.2V	1.5V



8111B 07/07/03

1. Correct circuit for 8111C..Add choke and output E/C cap for integrate switching power.
2. remove dummy circuit and 簡化

External Connection

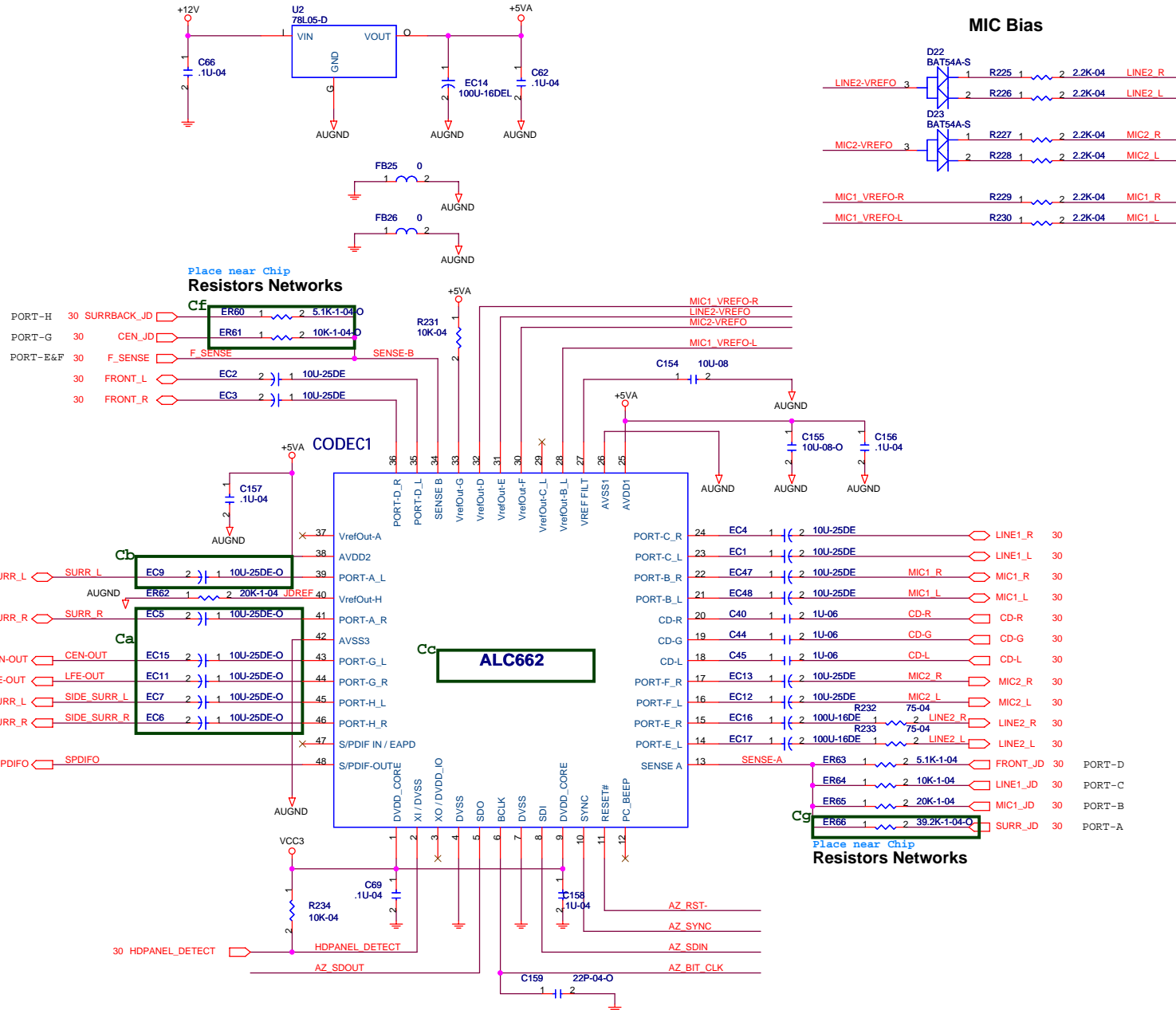


When you found some bug, please inform Ren(ext:665) to update circuit.

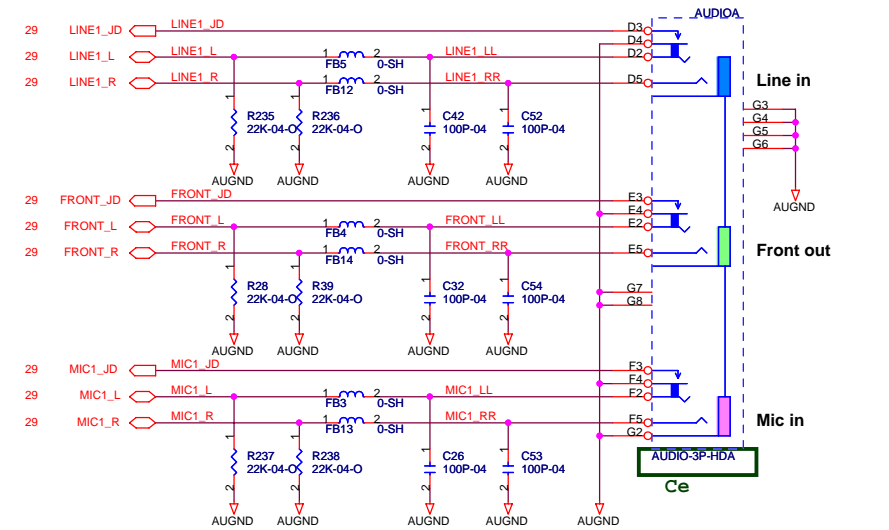
BOM Difference

Location	ALC883 7.1 Ch	ALC662 5.1 CH
Ca	V	X
Cb	V	X
Cc	ALC883	ALC662
Cd	V	X
Ce	AUDIO-6P	AUDIO-3P-HDA
Cf	V	X
Cg	V	X

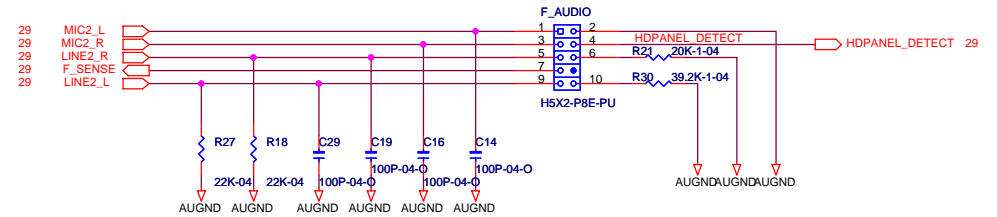
When you change BOM, remember change GPI to inform BIOS use different Verb-Table.



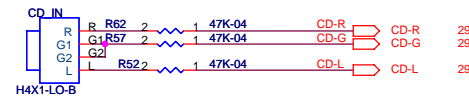
REAR-AUDIO



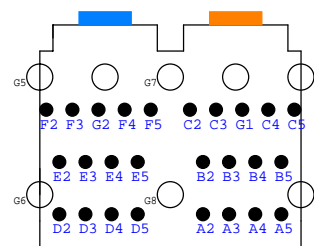
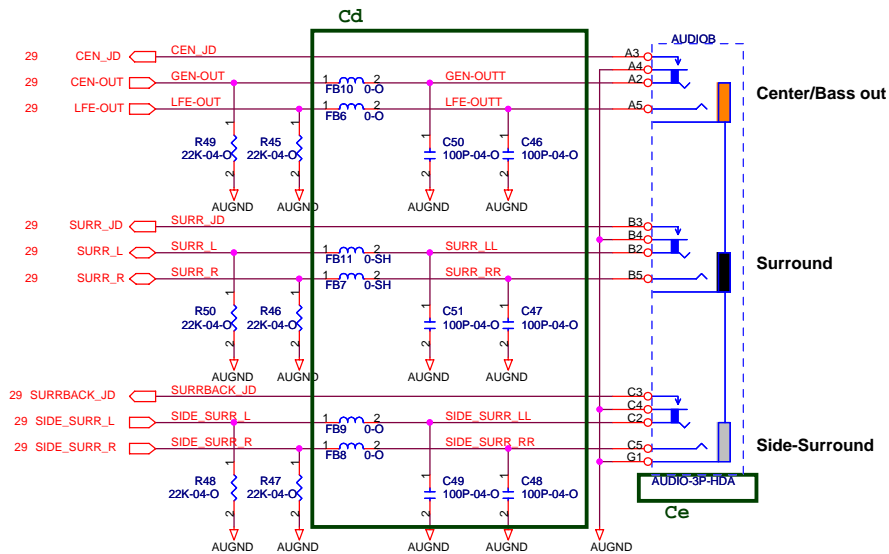
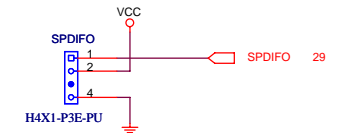
FRONT-AUDIO



CD_IN



SPDIF-OUT



TOP VIEW

